IN THE UNITED STATES PATENT OFFICE

Applicants:

David A. Knol et al.

Assignee:

Xilinx, Inc.

Title:

"System for Representing the Logical and Physical Information of an Integrated

Circuit"

Serial No.:

10/792,164

File Date:

March 3, 2004

Examiner:

Naum B. Levin

Art Unit:

2825

Docket No.:

X-1862 US

Conf. No.:

3762

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P.O. Box 1450

Alexandria, Virginia 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicants bring to the attention of the Examiner the three (3) references listed in the attached Substitute for Form 1449A/PTO. A copy of the non-patent reference is enclosed herein.

This Information Disclosure Statement is being filed under 37 CFR 1.97(b) prior to the receipt of a first office action.

Citation of the above documents shall not be construed as an admission that the documents are necessarily prior art with respect to the instant invention. Citation of the above documents shall not be construed as a representation that a search has been made other than as described above. Also, the citation of the above documents shall not be construed as an admission that the information cited herein is, or is considered to be, material to patentability as defined in §1.56(b).

No Fees are due however, the Commissioner is hereby authorized to charge any additional fees, or credit any overpayment which may be required to Deposit Account No. 24-0040.

Respectfully submitted,

Kim/Kanzaki, Ph.D. Attorney for Applicants Reg. No. 37,652

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on May 6, 2005.

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Substitute for form 1449A/PTO				Complete if Known			
Substitute to	or torm 1448	AVPIU		Application / Conf. No.	10/792,164 / 3762		
INFORMATION DISCLOSURE				Filing Date	March 03, 2004		
STATEMENT BY APPLICANT			PLICANT	First Named Inventor	David A. Knol		
			LIOAIII	Art Unit	2825		
(use as many sheets as necessary)		Examiner Name	Naum B. Levin				
Sheet	1	of	2	Attorney Docket Number	X-1862 US		

	U.S. PATENT DOCUMENTS						
Examiner Initials *	Cite No.1	Document Number Number - Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
muais	INO.	US- 6,170,080 B1	01-02-01	Ginetti et al.	Figures Appear		
	************	US- 6,408,422 B1	06-18-02	Hwang et al.			
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	FOREIGN PATENT DOCUMENTS								
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¹ Applicant's unique citation designation number (optional).² See Kinds of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ¹ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁵ Applicant is to place a check mark here if English language Translation is attached.

PTO/SB/08A (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
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(us				Examiner Name	Naum B. Levin	
Sheet	2	of	2	Attorney Docket Number	X-1862 US	

OTHER NON PATENT LITERATURE DOCUMENTS				
Examiner Initials *	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²	
		WANG, MAOGANG et al., "Multi-Million Gate FPGA Physical Design Challenges" ICCAD 2003, November 11-13, 2003, pp. 891-898, available from Cadence Design Systems, www.cadence.com, 2655 Seely Avenue, San Jose, California 95134		
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^{&#}x27;Applicant's unique citation designation number. 2 Applicant is to place a check mark here if English language Translation is attached.